






Method of plasma etching microminiature devices

Patent number: GB2098931
Publication date: 1982-12-01
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Classification:
- international: C09K13/00; H01L21/44
- european: H01L21/28E2B2P4, H01L21/3213C4B2
Application number: GB19820014402 19820518
Priority number(s): US19810266433 19810522

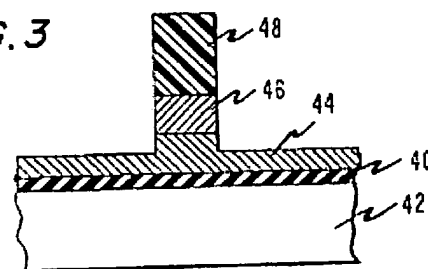
Also published as:

 NL8202103 (A)
 JP57198633 (A)
 FR2506519 (A1)
 DE3219284 (A1)
 BE893251 (A)

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Abstract of GB2098931

An advantageous low-resistivity gate-level metallization for VLSI MOS devices comprises TaSi₂ (46) on polysilicon (44). The two-layer composite overlies a relatively thin gate oxide film (40). In accordance with this invention, the two-layer composite is anisotropically patterned in a two-step reactive ion etching process. Patterning is carried out before the layers are sintered. In the preferred embodiment, CCl₃F is utilized to etch the TaSi₂ layer and some of the underlying polysilicon layer. Thereafter, utilizing Cl₂, the remaining polysilicon is etched in a step characterized by high selectivity with respect to the underlying gate oxide film.

FIG. 3

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